IN THE DRAWINGS:

The attached sheets of drawings include the changes to Fig. 3B that were indicated on page 2 of the Office Action. Replacement sheets are also attached for Figs. 3C, 8, 9 and 10, which now set forth formal lettering and numbering instead of handwritten lettering and numbering.

REMARKS

Claims 1-26 are pending in this application. Claims 1, 3, 4, 6, 9, 11, 14, 17, 18 and 19 were rejected under 35 U.S.C. 102(e) as being allegedly anticipated by U.S. Patent No. 7,043,569 ("Chou"). Applicants' attorney appreciates the indication that claims 2, 5, 7, 8, 10, 12, 13, 15, 16, and 20-26 would be allowable if re-written in independent form, including all of the limitations of the base claim and any intervening claims.

The specification has been amended as indicated on page 3 of the Office Action and to correct a typographical error. Claim 1 has been amended in order to correct a typographical error. Claim 2 has been amended to clarify the "JTAG" reference of claim 10 ("Joint Test Action Group ("JTAG") standard"). Claim 10 has been amended in response to the objection set forth on page 3 of the Office Action. The attached sheets of drawings include the changes to Fig. 3B that were indicated on page 2 of the Office Action. Replacement sheets are also attached for Figs. 3C, 8, 9 and 10, which now set forth formal lettering and numbering instead of hand-drawn lettering and numbering. No new matter has been added by way of these amendments. However, the rejections of Claim 1-26 are respectfully traversed, for the reasons cited below.

Responses to Claim Rejections

The Office Action asserts that Chou anticipates every element of claims 1 and 14. It is respectfully submitted, however, that there are several recitations of claims 1 and 14 that are not taught, indicated or suggested by Chou.

Some recitations of claims 1 and 14 that are not taught, suggested or indicated by Chou involve the existence of point-to-point intra-cluster links. For example, claim 1 recites the following:

> A computer system comprising a plurality of processor clusters, each cluster including a plurality of nodes, *the nodes including a processor and an interconnection controller interconnected by point-to-point intra-cluster links* . . . . [Emphasis added.]

Claim 14 recites the following:

> An interconnection controller for use in a computer system comprising a plurality of processor clusters, each cluster including a plurality of nodes, *the nodes including processors and an instance of the interconnection controller interconnected by point-to-point intra-cluster links* . . . . [Emphasis added.]

One example of a processor cluster having nodes connected by point-to-point intra-cluster links is shown in Fig. 2 of the present invention:

> Fig. 2 is a diagrammatic representation of a multiple processor cluster such as, for example, cluster 101 shown in Fig. 1A. Cluster 200 includes processors 202a-202d, one or more Basic I/O systems (BIOS) 204, a memory subsystem comprising memory banks 206a-206d, *point-to-point communication links 208a-208e,* and a service processor 212. The point-to-point communication links are configured to allow interconnections between processors 202a-202d, I/O switch 210, and interconnection controller 230.

(Id. at page 10, lines 11-16 [emphasis added].)

It is respectfully submitted that Chou does not teach point-to-point links within nodes (such as individual processors) of a cluster. With regard to these recitations, the Office Action references Fig. 1 of Chou, which displays devices including multiple processors. Each of the devices is connected through a switch fabric, which in turn is made up of multiple switches.

However, Fig. 1 of Chou does not indicate how processors or other nodes within such a device are connected. Chou does not describe such multi-processor devices in detail, but instead focuses on the configuration and functionality of switches, which Chou refers to as "interconnect devices." As shown in Fig. 2 of Chou, each switch uses internal bus 202 as opposed to a point-to-point connection.

Such bus-based, broadcast communications between nodes (such as processors) in a device differ from the point-to-point communications between nodes described in the present invention, as noted in the Background section:

A relatively new approach to the design of multi-processor systems replaces broadcast communication among processors with a point-to-point data transfer mechanism in which the processors communicate similarly to network nodes in a tightly-coupled computing system. That is, the processors are interconnected via a plurality of communication links and requests are transferred among the processors over the links according to routing tables associated with each processor. The intent is to increase the amount of information transmitted within a multi-processor platform per unit time.

(Id. at page 1, lines 16-22.)

Another element not taught, suggested or indicated by Chou involves the following recitations of claim 1:

A computer system comprising a plurality of processor clusters ... each of the *processors* [emphasis added] and the interconnection controller in a cluster having a test interface for communicating with the service processor ...

One example of a processor cluster having nodes (including a service processor) connected by point-to-point intra-cluster links is shown in Fig. 2 of the present invention:

The service processor 212 is configured to allow communications with processors 202a-202d, I/O switch 210, and interconnection controller 230 via a JTAG interface represented in Fig. 2 by links 214a-214f. It should be noted that other interfaces are supported. I/O switch 210 connects the rest of the system to I/O adapters 216 and 220, and to BIOS 204 for booting purposes.

Service processor 212 is primarily responsible for partitioning the resources of cluster 200. According to some embodiments, service processor 212 allocates usage of processor 202a-202d and I/O switch 210 although service processor 212 could be programmed to manage directly other resources such as, for example, memory banks or various I/O devices.

(Id. at page 10, line 16 to page 11, line 1.)

In rejecting claim 1, the Office Action asserts that this feature is taught by Fig. 2, column 4, lines 1-7 in Chou. Fig. 2 is a diagram for a switch. Lines 1-7 describe a management port module in the switch that can provide different components of the switch with configuration data. The management port module can incorporate a configuration module, which in turn receives commands from a processor coupled with each switch (see Fig. 3 of Chou.) As understood, neither these nor any other parts of Chou teach, suggest or indicate processors within a cluster communicating with, and being updated by, a service processor.

Other recitations of claims 1 and 14 that are not taught, suggested or indicated by Chou involve a node that is configured to inject the commands into a queue of pending commands according to an intra-cluster transaction protocol. For example, claim 1 recites "at least one of the nodes in a cluster is a command-injecting node configured to receive a command via a test interface and to inject the command into a queue of commands according to the intra-cluster transaction protocol." Similarly, claim 14 recites "the interconnection controller configured to receive commands via a test interface and to inject the commands into a queue of pending commands according to the intra-cluster transaction protocol."

In rejecting this part of claim 1, the Office Action refers to Fig. 3A and paragraph 5, lines 13-24 of Chou. Fig. 3A displays a processor subsystem for a switch. Lines 13-24 describe how the processor subsystem can send configuration data throughout the components of the switch.

The aforementioned text and diagram do not provide for the ability to queue commands. Figs. 4 and 5 are flow diagrams that describe the steps of the configuration process. No mention is made of a queue. The flow diagrams indicate that configuration commands are immediately implemented, as long as the configuration data are available. Queues, on the other hand, may involve the storage, delaying and/or prioritization of commands. As understood, Chou cannot anticipate claim 1 or claim 14 because Chou does not teach, suggest or indicate queues in relation to the issuance of commands.

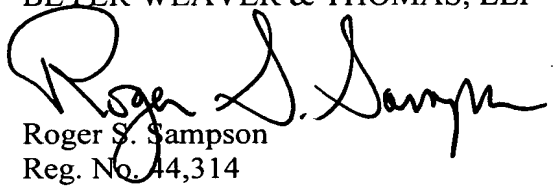
For at least the foregoing reasons, it is respectfully submitted that Chou does not anticipate claim 1 or claim 14, the only independent claims of this application. As a result, it is respectfully submitted that all pending claims are allowable.

CONCLUSION

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

The Commissioner is hereby authorized to charge any additional fees, including any extension fees, which may be required or credit any overpayment directly to the account of the undersigned, No. 50-0388 (Order No. NWISP029).

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



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